Amendments to the Specification

Detailed Description of the Preferred Embodiments

As previously noted, state-of-the-art resistive memory arrays require active devices, such as a diode or a transistor, to prevent interaction among the memory cells of the array. Thus, for a three-dimensional array, a polycrystalline diode, or transistor, is required for each cell, which is generally located above the first layer in the memory array. Polycrystalline diodes and polycrystalline transistors exhibit high leakage current, and therefore are not suitable for incorporation into large arrays. The polycrystalline layer may be crystallized to improve active device performance and reduce leakage current, however, the high temperature process required for crystallization may destroy the memory elements which are located under the polycrystalline layer. This invention solves this problem by providing a resistor memory cell which does not have an active device.

Referring now to Fig. 1, steps for fabricating the device of the invention, as shown in Fig. 1, generally at 10, include, initially, following any state-of-the-art processes to prepare a silicon substrate, 12, and fabrication of peripheral circuits, 14, on the silicon substrate. A first layer of silicon oxide, having a thickness of between about 100 nm to 1000 nm, is deposited and planarized, 16, by a chemical-mechanical polishing (CMP) process. A bottom electrode having a thickness of between about 50 nm to 300 nm of Pt, or a thickness of between about 10nm to 200nm of TiN and between about 10 nm to 100 nm of Pt, in a bi-layer electrode, is deposited and etched, 18. Materials for the bottom electrode may include Pt, $PtRhO_x$ $PtIrO_x$ and TiN/Pt. A second oxide layer having a thickness of at least 1.5X that of the thickness of the bottom electrode is deposited and ~~plainarized~~ planarized, 20, to a level where at the bottom electrode is exposed. Memory resistor material, such as a colossal magneto resistive (CMR) material, or other suitable